

Amendments to the Claims:

The following listing of the claims replaces all previous listings.

1 1 (Currently Amended). A monolithically integrated vertical PIN
2 photodiode formed in ~~biCMOS~~ BICMOS technology and having a substantially
3 planar surface facing the light and having a back side and anode terminals via
4 p regions on a topside of the photodiode, wherein an i-zone of the PIN
5 photodiode is formed by:

6 (a) a combination of a first p⁻ epitaxial layer with a thickness of
7 substantially 15μm at most and having a dopant concentration of less than
8 $5 * 10^{14} \text{ cm}^{-3}$, wherein the p⁻ epitaxial layer is located on a p substrate;

9 (b) a slightly doped n⁻ epitaxial second layer adjacent to the first
10 layer and having a dopant concentration in a range of substantially 10^{14} cm^{-3}
11 to 10^{15} cm^{-3} , wherein ~~the an~~ n⁺ cathode of the PIN photodiode is incorporated
12 into the second layer; and

13 wherein, in lateral direction, said p regions delineate the second n
14 epitaxial layer, and in addition to the anode terminals, a further anode contact
15 area of the PIN diode is provided at the back side.

1 2 (Currently Amended). The PIN photodiode of claim 1, wherein
2 buried p⁺ layers extending into the ~~[[p]]~~ p⁻ epitaxial layer are located below the
3 p regions which border the second n epitaxial layer in the lateral direction.

1 3 (previously presented). The PIN photodiode of claim 1, wherein at
2 least within the further anode contact area, acting as a back side, a silicon
3 wafer bearing the photodiode is thinned.

1 4 (previously presented). The PIN photodiode of claim 1 wherein the
2 anode of the PIN photodiode is electrically contacted from the frontside only.

1 5 (original). The PIN photodiode of claim 4, wherein one or
2 more anode terminals are formed by deep trench contacts.

1 6 (previously presented). The PIN photodiode of claim 1, wherein the
2 slightly doped n⁻ epitaxial layer has a dopant concentration of approximately
3 10¹⁴ cm⁻³.

1 7 (previously presented). The PIN photodiode of claim 1, wherein the
2 dopant concentration of the first epitaxial layer is substantially 10⁺¹³ cm⁻³.

1 8 (Currently Amended) The PIN photodiode of claim 1, wherein the
2 p regions are configured as p wells in a vertical section.

1 9 (Currently Amended) The PIN photodiode of claim 8, wherein the
2 wells extend to the first layer.

1 10 (Currently Amended). The PIN photodiode of claim 1, wherein a
2 dopant concentration of the second layer is less than a dopant concentration
3 of an n region in the second layer, wherein the n region forms the a collector
4 doping for contacting a cathode.

1 11 (previously presented). The PIN photodiode of claim 1, wherein
2 within and spaced apart from the p regions, a cathode region is provided.

1 12 (Currently Amended). A method for forming a monolithically
2 integrated vertical PIN photodiode according to a ~~biCMOS~~ BICMOS
3 technology, wherein:

4 (i) a p⁺ silicon wafer having a p⁻ epitaxial layer with a maximum
5 thickness of substantially 15µm and having a dopant concentration of
6 approximately 10¹³ cm⁻³ is used as base material;

7 (ii) after a subsequent implementation of a buried layer ~~a following n~~
8 an n⁻ epitaxial layer having a dopant concentration within a range of
9 approximately 10^{14} cm^{-3} is one of deposited and incorporated; and

10 (iii) thereafter, n and p wells are formed and standard following
11 process steps of the technology are performed, wherein in the n⁻ epitaxial
12 layer an n⁺ cathode of the PIN photodiode is incorporated, and in a lateral
13 direction p regions delineate the ~~[[n]]~~ n⁻ epitaxial layer and wherein in addition
14 to anode terminals via the p regions of the a planar top side a further anode
15 contact area is formed on the back side.

1 13 (Original). The method of claim 12, wherein finally the silicon
2 wafer at least within the area of the PIN diode is thinned at the back side with
3 a protective covering formed on the front side.

1 14 (Original). The method of claim 12, wherein the anode contact
2 area of the back side is not particularly formed and is not electrically
3 contacted.

1 15 (Currently Amended). The method of claim 12, wherein the back
2 side anode of a chip provided after dicing of the substrate ~~can is~~ is electrically be
3 contacted by attaching the chip to a lead frame or a conductive area of a
4 wiring board by means of a conductive adhesive, if the serial resistance is not
5 sufficient.

1 16 (Currently Amended). A monolithically vertical PIN photodiode
2 formed in biCMOS-BICMOS technology, wherein an i-zone of the PIN diode is
3 formed by the combination of a slightly doped p⁻ epitaxial layer having a
4 thickness up to substantially 15 μm with a dopant concentration of less than $5 \cdot$
5 10^{14} cm^{-3} and being located on a highly doped p⁺ substrate, with a slightly
6 doped n⁻ epitaxial layer formed adjacent to the p⁻ epitaxial layer and having a

7 dopant concentration in the range of approximately 10^{14} cm^{-3} , as range of
8 dopant concentration $\leq 10^{14} \text{ cm}^{-3}$ to $< 10^{15} \text{ cm}^{-3}$, into which the n^+ cathode of
9 the PIN photodiode is incorporated, wherein p regions laterally delineate the
10 ~~[[n]]~~ n^- epitaxial layer in lateral direction and wherein in addition to the anode
11 terminals, via the p well regions of the planar front side, a further anode
12 contact area of the PIN diode is provided at the back side ~~via the p well~~
13 ~~regions of the planar front side~~.

1 17 (previously presented). The monolithically integrated vertical PIN
2 photodiode of claim 16, wherein the range of dopant concentration is
3 substantially 10^{13} cm^{-3} .

1 18 (Currently Amended). The monolithically integrated vertical
2 PIN photodiode of claim 16, ~~characterized in that wherein~~ buried p^+ layers
3 ~~extending~~ extend into the p epitaxial layer and are located below the p
4 regions, which laterally delineate the slightly doped n^- ~~[[n]]~~ epitaxial layer in
5 lateral direction.

1 19 (Currently Amended). The monolithically integrated vertical
2 PIN photodiode of claim 16, characterized in that at least within the back side
3 anode~~[[,]]~~ the silicon wafer is thinned.

1 20 (original). The monolithically integrated vertical PIN
2 photodiode of claim 16, characterized in that the anode of the PIN photodiode
3 is electrically contacted from the front side only.

1 21 (original). The monolithically integrated vertical PIN
2 photodiode of claim 20, wherein one or more anode terminals are formed by
3 deep trench contacts.

1 22 (Currently Amended) A method of forming a monolithically
2 integrated vertical PIN photodiode in biCMOS-BICMOS technology, wherein:

3 (i) a p⁺ silicon wafer having formed thereon a p⁻ epitaxial layer with
4 a thickness of approximately 15μm and having a dopant concentration of
5 approximately 10¹³ cm⁻³ is used as an initial material;

6 (ii) after the a subsequent implementation of the a buried layer, the
7 ~~[[n]]~~ an n⁻ epitaxial layer subsequently formed is deposited according to a
8 standard process flow ~~is deposited with a dopant concentration having of~~
9 about 10¹⁴ cm⁻³; and

10 (iii) thereafter, ~~the n and p wells are formed~~ and all further standard
11 subsequent process steps of the technology are performed, wherein the n⁺
12 cathode of the PIN photodiode is incorporated into the n⁻ epitaxial layer,
13 wherein in lateral direction p regions laterally delineate the ~~[[n]]~~ an n⁻ epitaxial
14 layer and wherein in addition to anode terminals, via the p well regions of the
15 planar front side, a further anode contact area of the PIN diode is formed on
16 the back side, via the p well regions of the planar front side such that said
17 further anode contact area of the chip obtained after the dicing of the substrate
18 can be contacted by attaching the chip to a lead frame or a conductive area of
19 a wiring board by means of a conductive adhesive, to support a sufficiently
20 small serial resistance.

1 23 (Original). The method of claim 22, wherein in that in a final step the
2 silicon wafer is thinned at the back side at least within the PIN diode with the
3 front side being covered by a protective covering.

1 24 (Original). The method of claim 22, wherein the anode contact area
2 on the back side not particularly being formed and not electrically being
3 contacted.

1 25 (Currently Amended). The PIN photodiode of claim 1,
2 wherein the p⁻ epitaxial layer is located on a highly doped ~~[[p]]~~ p⁺ substrate.

1 26 (Currently Amended). The PIN photodiode of claim 2,
2 wherein the p regions are configured as p wells ~~in a vertical section and~~
3 wherein the p wells extend to the buried layer.